REMARKS

The present Preliminary Amendment is to make minor editorial revisions to the specification. It is submitted that these changes do not constitute new matter.

Attached hereto is a marked-up version of the changes made to the specification by the current Preliminary Amendment. The attached page is captioned "**Version With Markings to Show Changes Made**".

Respectfully submitted,

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1, a digital phase locked loop (digital PLL) 2, and an automatic equalizer 9. The automatic equalizer 9 is further constituted by a transversal filter 4 and a control unit 5.

The analog/digital converter 1 samples an analog reproduction signal which is input to the reproduction signal processor into the digital reproduction signal with a large number of values. The digital phase locked loop 2 generates a reference clock CK which coincides with the phase included in the digital reproduction signal and the reference frequency component. The transversal filter 4 performs waveform equalization of the digital reproduction signal. The control unit 5 controls a tap coefficient as a parameter of the transversal filter 4 by using an equalization error which is an error between the equalized waveform output from the transversal filter 4 and an equalization target value estimated from the equalized waveform, and the digital reproduction signal which is input to the transversal filter 4, such that the equalization error becomes minimum.

Next, an operation of the conventional reproduction signal processor will be described with reference to figure 7.

The digital information which is recorded on a recording medium is read by a scan of a head not shown, and the read signal is subjected to a processing for emphasizing a predetermined frequency band to result in an analog reproduction signal, which is input to the analog/digital converter 1 to be converted to

a multi-value digital reproduction signal. Then, the digital reproduction signal is input to both of the digital phase locked loop 2 and the transversal filter 4 of the automatic equalizer 9. The digital phase locked loop 2 extracts the reference clock CK by the input digital reproduction signal, and inputs the reference clock CK to the analog/digital converter 1 and the automatic equalizer 9. The reference clock CK is used as an operation clock in the analog/digital converter 1 and the automatic equalizer 9. On the other hand, the digital reproduction signal input to the transversal filter 4 is transmitted to a decoding circuit after the equalization in the transversal filter 4. In the equalization, the transversal filter 4 is controlled by the tap coefficient as its parameter. The tap coefficient is set from the input digital reproduction signal to the transversal filter 4 and an equalization error which is an error between an output signal from the transversal filter 4 and an equalization target value estimated on the basis of the output signal, in the control unit 5 at appropriate timings. Typically, in the control unit 5, an LMS algorithm for consecutively performing operations on the basis of a steepest descent method so that the square mean of equalization ~~target values~~ error becomes the minimum, is used.

Here, a setting method of the equalization target value will be described. The equalization target value is one for setting the frequency characteristics of the equalizer (FIR

The frequency divider 3 subjects the reference clock CK extracted by the digital phase locked loop 2 to frequency dividing process for performing integral multiplication of the period of the reference clock CK. The straight-line interpolation unit 6 is composed of a flip-flop element not shown and an adder. In the sampling in the analog/digital converter 1, the interpolation is performed for compensating the omission of the sampling number due to using the frequency-divided clock CK/N in place of the reference clock CK.

Next, the operation of the reproduction signal processor will be described with reference to figure 1.

The digital information which is recorded on a recording medium is read by a scan of a head not shown, and the read signal is subjected to a processing for emphasizing a predetermined frequency band to result in an analog reproduction signal, which is input to the analog/digital converter 1 to be converted to a multi-value digital reproduction signal. Then, the digital reproduction signal is input to both of the digital phase locked loop 2 and the transversal filter 4 of the automatic equalizer 8. The digital phase locked loop 2 extracts the reference clock CK by the input digital reproduction signal, and inputs the reference clock CK to the frequency divider 3. The frequency divider 3 performs frequency dividing process for performing integral multiplication of the period of the reference clock

CK, and outputs a frequency-divided clock CK/N. The frequency-divided clock CK/N is used as the operation clock in the analog/digital converter 1 and the automatic equalizer 8. Here, N denotes the division ratio, and the frequency-division ratio is referred to as N=2 in this first embodiment (hereinafter, referred to as "2-frequency-division"). On the other hand, the digital reproduction signal input to the transversal filter 4 is transmitted to a decoding circuit after the equalization in the transversal filter 4. In the equalization, the transversal filter 4 is controlled by the tap coefficient as the parameter. The tap coefficient is set from the digital reproduction signal input through the transversal filter 4, and an equalization error which is an error between an output signal from the transversal filter 4 and an equalization target value, in the control unit 5 at approximate timings. Typically, in the control unit 5, an LMS algorithm for consecutively performing operations on the basis of a steepest descent method so that the square mean of equalization ~~target values~~ error becomes the minimum, is used. As for the equalized waveform output from the transversal filter 4, by using the frequency-divided clock CK/N as the operation clock, the sampling number gets less than that in the case of using the reference clock CK. Thereby, in order to prevent the setting of the equalization target value in the control unit 5 from becoming unstable, the output equalized waveform of the

transversal filter 4 is input to the control unit 5, and as well as the straight-line interpolation unit 6 performs interpolation in the output equalized waveform, the signal obtained by interpolating the samples which are omitted due to using the frequency-divided clock CK/N is also input to the control unit 5. Thereby, the setting of the equalization target value can be performed with stability, similarly as in the case of using the reference clock CK.

Next, a straight-line interpolation will be described with reference to waveform charts, figures 2(a)-2(c) and figures 3(a)-3(c).

Figures 2(a)-2(c) and figures 3(a)-3(c) show an example of the digital reproduction signal, the equalized waveform, and the waveform obtained by performing the straight-line interpolation in the equalized waveform.

Figure 2(a) is a diagram showing an example of the digital reproduction signal, and ◇ shows the point obtained by sampling the analog reproduction signal by using the 2-frequency-divided clock (hereinafter, referred to as "a sampling point"). Figure 2(b) is a diagram showing the equalized waveform obtained by equalizing the digital reproduction signal in figure 2(a) by the transversal filter 4, and ◇ shows the sampling point after the waveform equalization. Figure 2(c) is a diagram showing the equalized waveform (an ideal waveform) in the case of using the reference clock, and ◇ shows the sampling point in the case